In the Claims:

1-5. cancelled

6. (new) An integrated circuit comprising:

A. logic circuitry having groups of logic stimulus inputs and logic response outputs;

B. a scan in lead;

C. a first scan path segment having scan stimulus outputs connected to a first group of logic stimulus inputs, scan response inputs connected to the first group of logic response outputs, a scan input coupled to the scan in lead, a scan enable input, a scan clock input, and an output buffer having a scan output;

D. a cache bit memory having a data input and a data output connected in series between the scan in lead and the scan input of the first scan path, the cache bit memory having a scan clock input connected to the scan clock input of the first scan path segment;

E. a second scan path segment having scan stimulus outputs connected to a second group of logic stimulus inputs, scan response inputs connected to the second group of logic response outputs, a scan input connected to the scan in lead, a scan enable input, a scan clock input, and an output buffer having a scan output; and

F. a scan out lead connected to the scan outputs of the first and second scan path output buffers.

7. (new) The integrated circuit of claim 6 in which the scan clock inputs of the first and second scan path segments are connected to separate clocking signals.

8. (new) The integrated circuit of claim 6 in which the cache bit memory is a D-type flip-flop.

9. (new) The integrated circuit of claim 6 in which the output buffers are 3-state buffers receiving separate enable signals.

10. (new) The integrated circuit of claim 6 including an additional scan path segment connected between the scan in lead and the scan out lead, with a second cache bit memory connected in series between the scan in lead and the additional scan path segment.

11. (new) The integrated circuit of claim 6 in which the cache bit memory contains one bit.

12. (new) The integrated circuit of claim 6 in which the cache bit memory is unconnected to the logic stimulus inputs and the logic response outputs.